REMARKS

In the foregoing amendments, claims 1 and 18 are amended. Claims 1-3, 5-11, 18, 21, and 23-30 remain pending in the present application.

I. Examiner Interview

Applicants wish to thank Daniel Cavallari and Brian Sircus for discussing the present application and outstanding Office Action with Applicant's representative during a telephone conversation on March 8, 2007. It is believed that certain issues were identified during the telephone conversation and that these issues have been resolved herein. During the conversation, the Examiners seemed to indicate that it would be beneficial for Applicants to make certain amendments to better place the present application in condition for allowance. Particularly, the Examiners seemed to indicate that claim amendments to clarify the distinction between a delayed output and one that is not delayed would better place this application in condition for allowance.

In addition, Applicant's representative mentioned during the telephone conversation that any amendment to the claim language regarding the aspect of a "delay" during an on-to-off transition at the output of the inverting switch would merely be a clarification of the claims. Such an amendment would not significantly change the intended scope of the claims. Therefore, it is believed that a further search would not be required of the Examiner and that a reconsideration of the amended claims of the present application can be made herein within the realm of normal prosecution of the present application. In this respect, it is respectfully requested that the Examiner kindly enter and reconsider the amended claims and pass the present application to issue.

II. Indication of Allowable Subject Matter

Applicants also wish to thank the Examiner for indicating the presence of allowable subject matter. In particular, claims 21 and 27-30 were indicated as allowable.

III. Response to 35 U.S.C. §102 Rejections

Claims 1-3 and 5 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by *Eitan et al.* (U.S. Patent No. 5,886,561). Applicants respectfully traverse this rejection on the grounds that *Eitan et al.* fail to disclose each and every element of independent claim 1, as amended.

In addition, claims 1, 6-11, 18, and 23-26 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by *Little et al.* (U.S. Patent No. 4,908,790). Applicants respectfully traverse this rejection on the grounds that *Little et al.* fails to disclose each and every element of independent claims 1 and 18, as amended.

A. Claims 1-3 and 5-11

Independent claim 1 is reproduced below:

1. A system comprising:

a threshold detector circuit;

a first switching circuit for enabling access to a back-up power source, the first switching circuit comprising at least a first transistor; and

an inverting switch coupled between the first switching circuit and the threshold detector circuit, the inverting switch comprising an input and an output, the inverting switch configured to receive a signal at the input, invert the signal, and provide the inverted signal from the output to the first switching circuit, ***the inverting switch further comprising a delay circuit, the delay circuit configured to provide a substantially-immediate high-output during an off-to-on transition at the output of the inverting switch and a switching delay during an on-to-off transition at the output of the inverting switch***;

wherein the threshold detector circuit is configured to cause the first switching circuit to enable access to the back-up power source responsive to a voltage provided by a primary power source dropping below a predetermined threshold.

(Emphasis added)

Eitan et al. and *Little et al.* each fail to particularly disclose every feature of claim 1, particularly the above-highlighted features. For example, claim 1 recites that the

inverting switch comprises ***a delay circuit, the delay circuit configured to provide a substantially-immediate high-output during an off-to-on transition at the output of the inverting switch and a switching delay during an on-to-off transition at the output of the inverting switch***. Assuming for the sake of argument that the inverter 22 of *Eitan et al.* is a conventional inverter, it is clear to one of ordinary skill in the art that conventional inverters do not comprise a ***delay circuit***. Furthermore, *Eitan et al.* does not disclose that the inverter 22 comprises a ***delay circuit*** as claimed in claim 1. In particular, the claimed delay circuit is ***configured to provide a substantially-immediate high-output during an off-to-on transition at the output of the inverting switch and a switching delay during an on-to-off transition at the output of the inverting switch***. *Eitan et al.* does not disclose a circuit capable of providing ***a substantially immediate high output*** during an off-to-on transition and ***a switching delay*** during an on-to-off transition.

Likewise, *Little et al.* also fails to disclose an inverting switch that comprises ***a delay circuit, the delay circuit configured to provide a substantially-immediate high-output during an off-to-on transition at the output of the inverting switch and a switching delay during an on-to-off transition at the output of the inverting switch***. Assuming for the sake of argument that the inverter 63 of *Little et al.* is a conventional inverter, it again is clear to one or ordinary skill in the art that conventional inverters do not disclose a delay circuit. Furthermore, *Little et al.* does not disclose that the inverter 63 comprises a ***delay circuit***, as claimed. Particularly, the claimed delay circuit is ***configured to provide a substantially-immediate high-output during an off-to-on transition at the output of the inverting switch and a switching delay during an on-to-off transition at the output of the inverting switch***, which *Little et al.* also fails to disclose.

For at least the reason that *Eitan et al.* and *Little et al.* fail to disclose each and every aspect of claim 1, it is believed that claim 1 is allowable over these cited references. In addition, claims 2, 3, and 5-11 are also believed to be allowable for at least the reason that they depend directly or indirectly from allowable independent claim 1.

B. Claims 18 and 23-26

Independent claim 18 is reproduced below:

18. A system comprising:

a threshold detector circuit;

a first switching circuit for enabling access to a back-up power source, the first switching circuit comprising at least a first transistor;

a second switching circuit for enabling access to a primary power source, the second switching circuit comprising at least one transistor;

an inverting switch coupled between the first switching circuit and the threshold detector, ***the inverting switch configured to provide a substantially instantaneous high output during an on-to-off transition at an input of the inverting switch and a delayed-off output during an off-to-on transition at the input of the inverting switch***; and

an inverter coupled between the inverting switch and the threshold detector circuit;

wherein the threshold detector circuit is configured to cause the first switching circuit to enable access to the back-up power source responsive to a voltage provided by the primary power source dropping below a predetermined threshold; and

wherein the threshold detector circuit is configured to cause the second switching circuit to enable access to the primary power source responsive to a voltage provided by the primary power source rising above the predetermined threshold.

(Emphasis added)

Little et al. fails to disclose the above-highlighted features of claim 18. For example, claim 18 recites an ***inverting switch configured to provide a substantially instantaneous high output during an on-to-off transition at an input of the inverting switch and a delayed-off output during an off-to-on transition at the input of the inverting switch***. Assuming for the sake of argument that the inverter 63 of *Little et al.* is a conventional inverter, the inverter 63 merely inverts a signal and does not provide a ***substantially instantaneous high output*** during an on-to-off transition and ***a delayed-off output*** during an off-to-on transition as claimed.

For at least this reason, it is believed that claim 18 is allowable over *Little et al.* In addition, claims 23-26 are believed to be allowable for at least the reason that they depend directly or indirectly from allowable independent claim 18.

CONCLUSION

Any other statements in the Office Action that are not explicitly addressed herein are not intended to be admitted. In addition, any and all findings of inherency are traversed as not having been shown to be necessarily present. Furthermore, any and all findings of well-known art and official notice, or statements interpreted similarly, should not be considered well known for at least the specific and particular reason that the Office Action does not include specific factual findings predicated on sound technical and scientific reasoning to support such conclusions.

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-3, 5-11, 18, 21, and 23-30 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned at (770) 933-9500.

Respectfully submitted,

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